Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A data carrier comprising a circuit, which circuit comprises the following components, namely

first memory means, which are designed for modifiable storage of information, the information being modifiable by an ambient parameter of the circuit, which ambient parameter acts on the first memory means, characterized in that the first memory means comprise a test memory area, which is provided for storing test information, wherein the first memory means comprises multiple data sectors and wherein the test memory area comprises data sector-specific test memory areas within each of the multiple data sectors, and

second memory means are provided which are designed for unmodifiable storage of reference information, and

detection means are provided, to which the test information which may be read out from the first memory means and the reference information which may be read out from the second memory means may be supplied and which are designed, with the aid of the read-out test information and the read-out reference information, to detect a modification of the originally stored test information brought about by an ambient parameter acting on the first memory means~~;~~

~~wherein the ambient parameter is one of a short-wave light, an electromagnetic field, and a high temperature~~.

2. (original) A data carrier as claimed in claim 1, characterized in that the detection means comprise comparison means for comparing the stored test information with the stored reference information.

3. (original) A data carrier as claimed in claim 1, characterized in that enabling means are provided for the purpose of irreversibly enabling functioning of the detection means, and the detection means are designed to cooperate with the enabling means.

4. (original) A data carrier as claimed in claim 1, characterized in that the detection means are designed to generate and output an indicator signal, which indicator signal is provided to indicate a modification of the originally stored test information brought about by an ambient parameter acting on the first memory means and the circuit is designed to influence its operating behavior as a function of the indicator signal.

5. (original) A data carrier as claimed in claim 1, characterized in that the test information is formed of at least two bits, which at least two bits differ from one another with regard to their logical value.

6. (currently amended) A circuit, which circuit comprises the following components, namely

first memory means, which are designed for modifiable storage of information, the information being modifiable by an ambient parameter of the circuit, which ambient parameter acts on the first memory means, characterized in that the first memory means comprise a test memory area, which is provided for storing test information, wherein the first memory means comprises multiple data sectors and wherein the test memory area comprises data sector-specific test memory areas within each of the multiple data sectors, and

second memory means are provided which are designed for unmodifiable storage of reference information, and

detection means are provided, to which the test information which may be read out from the first memory means and the reference information which may be read out from the second memory means may be supplied and which are designed, with the aid of the read-out test information and the read-out reference information, to detect a modification of the originally stored test information brought about by an ambient parameter acting on the first memory means;

wherein the ambient parameter is one of a short-wave light, an electromagnetic field, and a high temperature.

7. (original) A circuit as claimed in claim 6, characterized in that the detection means comprise comparison means for comparing the stored test information with the stored reference information.

8. (original) A circuit as claimed in claim 6, characterized in that enabling means are provided for the purpose of irreversibly enabling functioning of the detection means, and the detection means are designed to cooperate with the enabling means.

9. (original) A circuit as claimed in claim 6, characterized in that the detection means are designed to generate and output an indicator signal, which indicator signal is provided to indicate a modification of the originally stored test information brought about by an ambient parameter acting on the first memory means, and the circuit is designed to influence its operating behavior as a function of the indicator signal.

10. (original) A circuit as claimed in claim 6, characterized in that the test information is formed of at least two bits, which at least two bits differ from one another with regard to their logical value.

11. (original) A circuit as claimed in claim 6, characterized in that the circuit takes the form of an integrated circuit.

12. (previously presented) A data carrier as claimed in claim 4, wherein the detection means generates and outputs an indicator signal that provides a perpetual indication of the modification of the originally stored test information.

13. (previously presented) A circuit as claimed in claim 9, wherein the detection means generates and outputs an indicator signal that provides a perpetual indication of the modification of the originally stored test information.

14. (previously presented) A data carrier as claimed in claim 1, wherein the ambient parameter deletes the test information.

15. (previously presented) A data carrier as claimed in claim 1, wherein the ambient parameter renders the test information unusable.

16. (previously presented) A circuit as claimed in claim 9, wherein the ambient parameter deletes the test information.

17. (previously presented) A circuit as claimed in claim 9, wherein the ambient parameter renders the test information unusable.

18. (new) A data carrier as claimed in claim 1, wherein the data sector-specific test memory areas are located in an area of each data sector that is designated for access control.

19. (new) A circuit as claimed in claim 6, wherein the data sector-specific test memory areas are located in an area of each data sector that is designated for access control.